Amendments to the Claims

Please cancel claim 32. Please amend claims 4, 20, 24, 33 and 34. The currently pending claims after amendment are listed below.

1. (Original) A digital data processing device, comprising:

a memory, said memory containing a page table, said page table having a plurality of page table entries corresponding to addressable pages, wherein each of a plurality of said page table entries contains, for each of a plurality of cacheable sub-units of the corresponding addressable page, respective cacheable sub-unit reference history data;

at least one processor;

at least one cache for temporarily storing data from said memory; and

a pre-fetch engine, said pre-fetch engine pre-fetching selective cacheable sub-units of addressable pages to said at least one cache, said pre-fetch engine selecting cacheable sub-units of addressable pages for pre-fetching using said cacheable sub-unit reference history data.

2. (Original) The digital data processing device of claim 1, wherein said pre-fetch engine identifies a page for selective pre-fetching upon the occurrence of at least one pre-defined event with respect to said page, and responsive to identifying a page for selective pre-fetching, selects cacheable sub-units of the identified page for pre-fetching using said cacheable sub-unit reference history data.

3. (Original) The digital data processing device of claim 2, wherein said pre-defined event with respect to said identified page comprises loading address translation data for said page into an address translation cache structure.

4. (Currently Amended) The digital data processing device of claim 3, wherein said address translation cache structure is an ~~effective-to-real~~ effective-to-real address translation table (ERAT).

5. (Original) The digital data processing device of claim 1, wherein said reference history data comprises an up-or-down counter which is incremented on the occurrence of at least one pre-defined event of a first set and decremented on the occurrence of at least one pre-defined event of a second set.

6. (Original) The digital data processing device of claim 5, wherein said up-or-down counter is incremented if a respective cacheable sub-unit is loaded to said cache and referenced while in said cache, and decremented if the respective cacheable sub-unit is loaded to said cache and not referenced while in said cache.

7. (Original) The digital data processing device of claim 1, wherein said digital data processing device comprises a plurality of caches at a plurality of cache levels, and wherein said pre-fetch engine pre-fetches data to different cache levels.

8. (Original) The digital data processing device of claim 1, wherein said digital data processing system comprises:

a plurality of processors;

a plurality of caches at a plurality of cache levels, wherein a first of said cache levels comprising a plurality of caches, each cache associated with a single respective processor, and wherein a second of said cache levels comprises at least one cache which is shared by a plurality of processors.

9. (Original) The digital data processing device of claim 1, wherein said digital data processing system further comprises:

an address translation mechanism which translates effective addresses in an address space of a task executing on said at least one processor to virtual addresses in a global address space of said digital data processing system, and translates said virtual addresses to real addresses corresponding to physical memory locations in said memory.

10. (Original) The digital data processing device of claim 9, wherein said pre-fetch engine further pre-fetches address translation data into at least one address translation cache structure of said address translation mechanism.

11. (Original) A method for pre-fetching data to at least one cache a digital data processing device, comprising the steps of:

maintaining, for each of a plurality of memory pages in a memory of said digital data processing device, at least one respective up-or-down counter, each said counter being incremented upon the occurrence of an event of a first type with respect to data in the memory page corresponding to the counter, and decremented upon the occurrence of an event of a second type with respect to data in the memory page corresponding to the counter; and

determining whether to pre-fetch data in a page of memory based on a value of said at least one up-or-down counter corresponding to the memory page.

12 (Original) The method for pre-fetching data of claim 11,

wherein said step of maintaining at least one up-or-down counter comprises maintaining, for each said memory page, a plurality of respective up-or-down counters in a page entry in a page table corresponding to the memory page, each up-or-down counter corresponding to a respective cacheable sub-unit of the memory page represented by the corresponding page entry in said page table, each said counter being incremented upon the occurrence of an event of said first type with respect to data in the cacheable sub-unit corresponding to the counter, and decremented upon the occurrence of an event of said second type with respect to data in the cacheable sub-unit corresponding tot he counter; and

wherein said step of determining whether to pre-fetch data in a page of memory comprises determining whether to pre-fetch a cacheable sub-unit of the page in memory based on a value of the up-or-down counter corresponding to the cacheable sub-unit.

13. (Original) The method for pre-fetching data of claim 12, wherein said cacheable sub-unit corresponds to the size of a cache line of at least one cache of said digital data processing device.

14. (Original) The method for pre-fetching data of claim 12, wherein said step of determining whether to pre-fetch data in a page comprises:

identifying a page for selective pre-fetching upon the occurrence of at least one event of a third type with respect to said page;

responsive to identifying a page for selective pre-fetching, selecting cacheable sub-units of the identified page for pre-fetching using said cacheable sub-unit reference history data.

15. (Original) The method for pre-fetching data of claim 14, wherein said pre-defined event with respect to said identified page comprises loading address translation data for said page into an address translation cache structure.

16. (Original) The method for pre-fetching data of claim 11,

wherein said event of said first type comprises loading said data into a cache of said digital data processing device, and referencing said data while it is in the cache; and.

wherein said event of said second type comprises loading said data into a cache of said digital data processing device, and casting said data out of said cache before it is referenced.

17. (Original) A processor for a digital data processing device, comprising:

an instruction unit determining instruction sequences;

an execution unit executing instructions in said instruction sequences;

at least one cache for temporarily storing data from a memory of said digital data processing device for use by at least one of said instruction unit and said execution unit;

a pre-fetch engine, said pre-fetch engine pre-fetching selective cacheable sub-units of addressable pages of said memory to said at least one cache, said pre-fetch engine selecting cacheable sub-units of addressable pages for pre-fetching using cacheable sub-unit reference history data obtained from said memory; and

reference history maintenance logic, said reference history maintenance logic updating said reference history data corresponding to each respective cacheable sub-unit in response to reference history events occurring in said processor with respect to the respective cacheable sub-unit.

18. (Original) The processor for a digital data processing device of claim 17, wherein said pre-fetch engine identifies an addressable page for selective pre-fetching upon the occurrence of at least one pre-defined event with respect to said addressable page, and responsive to identifying an addressable page for selective pre-fetching, selects cacheable sub-units of the identified addressable page for pre-fetching using said cacheable sub-unit reference history data.

19. (Original) The processor for a digital data processing device of claim 18, wherein said pre-defined event with respect to said identified addressable page comprises loading address translation data for said page into an address translation cache structure.

20. (Currently Amended) The processor for a digital data processing device of claim 19, wherein said address translation cache structure is an ~~effective-to-real~~ effective-to-real address translation table (ERAT).

21. (Original) The processor for a digital data processing device of claim 17, wherein said reference history data comprises an up-or-down counter which is incremented on the occurrence of at least one pre-defined event of a first set and decremented on the occurrence of at least one pre-defined event of a second set.

22. (Original) The processor for a digital data processing device of claim 21, wherein said up-or-down counter is incremented if a respective cacheable sub-unit is loaded to said cache and referenced while in said cache, and decremented if the respective cacheable sub-unit is loaded to said cache and not referenced while in said cache.

23. (Original) The processor for a digital data processing device of claim 17, wherein said pre-fetch engine further pre-fetches address translation data into at least one address translation cache structure of an address translation mechanism.

24. (Currently Amended) A digital data processing device, comprising:

at least one processor which generates memory references to memory address locations;

a memory, said memory containing a page table, said page table having a plurality of page table entries corresponding to addressable pages, wherein each of ~~a plurality~~ at least some of said page table entries contains persistent reference history data with respect to memory references generated by said at least one processor to memory address locations within the corresponding addressable page, said persistent reference history data being maintained throughout the life of the corresponding addressable page in memory;

at least one cache for temporarily storing data from said memory for use in satisfying said memory references generated by said at least one processor; and

a pre-fetch engine, said pre-fetch engine pre-fetching data from said addressable pages to said at least one cache, said pre-fetch engine selecting data for pre-fetching using said persistent reference history data.

25. (Original) The digital data processing device of claim 24, wherein said digital data processing system comprises a plurality of processors, and said persistent reference history data is based on reference events occurring in said plurality of processors.

26 (Original) The digital data processing device of claim 24,

wherein each said page table entry contains, for each of a plurality of cacheable sub-units of the corresponding addressable page, respective cacheable sub-unit reference history data; and

wherein said pre-fetch engine determines whether to pre-fetch a cacheable sub-unit of the page in memory based on the respective cacheable sub-unit reference history data..

27. (Original) The digital data processing device of claim 24, wherein said persistent reference history data comprises an up-or-down counter which is incremented on the occurrence of at least one pre-defined event of a first set and decremented on the occurrence of at least one pre-defined event of a second set.

28. (Original) The digital data processing device of claim 27, wherein said up-or-down counter is incremented if data in a respective addressable page is loaded to said cache and referenced while in said cache, and decremented if data in the respective addressable page is loaded to said cache and not referenced while in said cache.

29. (Original) The digital data processing device of claim 24, wherein said digital data processing device comprises a plurality of caches at a plurality of cache levels, and wherein said pre-fetch engine pre-fetches data to different cache levels.

30. (Original) The digital data processing device of claim 24, wherein said digital data processing system further comprises:

an address translation mechanism which translates effective addresses in an address space of a task executing on said at least one processor to virtual addresses in a global address space of said digital data processing system, and translates said virtual addresses to real addresses corresponding to physical memory locations in said memory.

31. (Original) The digital data processing device of claim 30, wherein said pre-fetch engine further pre-fetches address translation data into at least one address translation cache structure of said address translation mechanism.

32. (Cancelled) .

33. (Currently Amended) ~~The~~ A digital data processing device ~~of claim 32~~, comprising:

a plurality of processors;

a memory, said memory containing a page table, said page table having a plurality of page table entries corresponding to addressable pages, wherein each of at least some of said page table entries contains persistent reference history data with respect to the corresponding addressable page, said persistent reference history data containing reference history from said plurality of processors, wherein each said page table entry contains, for each of a plurality of cacheable sub-units of the corresponding addressable page, respective cacheable sub-unit reference history data;

at least one cache for temporarily storing data from said memory; and

a pre-fetch engine, said pre-fetch engine pre-fetching data from said addressable pages to said at least one cache, said pre-fetch engine selecting data for pre-fetching using said persistent reference history data, wherein said pre-fetch engine determines whether to pre-fetch a cacheable sub-unit of the page in memory based on the respective cacheable sub-unit reference history data.

34. (Currently Amended) ~~The~~ A digital data processing device ~~of claim 32~~, comprising:

a plurality of processors;

a memory, said memory containing a page table, said page table having a plurality of page table entries corresponding to addressable pages, wherein each of at least some of said page table entries contains persistent reference history data with respect to the corresponding addressable page, said persistent reference history data containing reference history from said plurality of processors, wherein said persistent reference history data comprises an up-or-down counter which is incremented on the occurrence of at least one pre-defined event of a first set and decremented on the occurrence of at least one pre-defined event of a second set;

at least one cache for temporarily storing data from said memory; and

a pre-fetch engine, said pre-fetch engine pre-fetching data from said addressable pages to said at least one cache, said pre-fetch engine selecting data for pre-fetching using said persistent reference history data.